# SDD Review Document

## Summary

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| --- | --- |
| **Date** | 4/August/2021 |
| **Effort** | 2 hrs |
| **Room/Location** | Personal |
| **Review Status** | Closed |
| **Review name** | SDD\_Door.doc |
| **Method** | Comments |
| **Release** | Initial |
| **Responsible** | Tania Lozoya |
| **Project** | Door Control Module |
| **Reason of Review** | New document |

## Comment List

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **No.** | **Reference** | **Comments / Actions** | **Classification (E)rror/Risk / (R)emark** | **Responsible person/Planned date for completion** | **Completion(Name/Date)** |
| 1 | Table of contents | Add new section items | Remark | Marco Antonio Mares |  |
| 2 | Abbreviations | Add ECU Electronic Control Unit | Remark | Marco Antonio Mares |  |
| 3 | Abbreviations | Add DIO Digital Input Ouput | Remark | Marco Antonio Mares |  |
| 4 | Abbreviations | Add HW Hardware | Remark | Marco Antonio Mares |  |
| 5 | Abbreviations | Add SW Software | Remark | Marco Antonio Mares |  |
| 6 | Section 5 | Add function description and dynamic behavior for Init function. | Risk | Marco Antonio Mares |  |
| 7 | Section 5 | Add function description and dynamic behavior for Run function. | Risk | Marco Antonio Mares |  |
| 8 | Section 5 | Add function description and dynamic behavior for Door\_Get\_Status function. | Risk | Marco Antonio Mares |  |

## Check List

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| No | Description | OK / NOK / NR | Comment | Responsible person /  Planned date for completion | Status |
| 1 | Does the design comply to the SW architecture? (interfaces, scheduling...) | OK |  |  | Closed |
| 2 | Are all requirements allocated to Desing elements? | NOK | DCU\_SWR\_137  DCU\_SWR\_138  DCU\_SWR\_139 | Marco Antonio Mares | Open |
| 3 | Are all operations described in an adequate detail and with the adequate notation? | NOK | Complete section for Init, Run and Door\_Get\_Status | Marco Antonio Mares | Open |
| 4 | Is the coupling level between SW parts (internal or externals) reduced to the minimum?  Is the justification of all global data written in the design document? | OK |  |  | Closed |
| 5 | Is each data owned by one unit?  If a data is public (for read and/or for write operations), is its access made using a method provided by the owner?  (if a method is provided for read and write operations on the same pubilc data, the data has to be private) | OK |  |  | Closed |
| 6 | How are the variables initialized? If not initialized, is the reason explained? | NOK | Detail information for Init | Marco Antonio Mares | Open |
| 7 | Is the mechanism to initialise the functionality (when needed) described?  (eg: function calls, data acquisition …) | NOK | Detail information for Init | Marco Antonio Mares | Open |
| 8 | In case of global variable (shared or not shared) used in reentrance function (reentrance raised by an ISR), is there a mechanism to avoid data modification during its treatment? | NR |  |  | Closed |
| 9 | Are Tasks, ISRs and event notification function kept as short as possible? | OK |  |  | Closed |
| 10 | Is the state variable only used in one single module?  (If the state variable needs to be visible from another module (to be avoided), indicate it in the design and use the mechanism of read copy on that variable). | OK |  |  | Closed |
| 11 | Is the event memorization (ex: flag) consumed at the end of each reccurence of a state machine?  Otherwise, the risk is to use an obsolete event (ex: event memorization consumption conditionned by a state transition). | NR |  |  | Closed |
| 12 | In case of asynchronous reception of the same event by several objects (ex: state machine, C function called periodicly…), has each object its own memorization mechanism (ex: separate flags). | NR |  |  | Closed |